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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,099	10/21/2003	Mitsuhiro Kanayama	01-486	8953

23400 7590 10/29/2004

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EXAMINER	
RAO, SHRINIVAS H	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 10/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/689,099	KANAYAMA ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/21/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of paper submitted under 35 U.S.C. 119(a)-(d), claiming priority from Japanese Patent Application No. 2002-305632 filed on October 21, 2002 which papers have been placed of record in the file.

Information Disclosure Statement

Acknowledgment is made of receipt of Applicant's Information Disclosure Statement (PTO-1449) filled on 10/ 21/ 2003.

The references on PTO 1499 submitted on 10/21/2003 are acknowledged. All the cited references have been considered. However the foreign patents and documents cited by applicant are considered to the extent that could be understood from the abstract and drawings.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakano (U.S. Patent No. 5,616,952, herein after Nakano) .

With respect to claim 1 Nakano describes an electronic control device having a power supply circuit formed on a multi-layered substrate for adjusting a power supply

voltage supplied by an external power supply to a desired level, the power supply circuit including a switching component to which the power supply voltage is applied at an input terminal thereof and which is driven by a duty signal and an output voltage forming circuit for producing an output voltage formed from a voltage inputted from the switching device, comprising :

a ground wiring pattern dedicated for the output forming circuit; (Nakano figure 2 A col. 3 lines 65-67)a common ground wiring pattern for all electronic circuits included in the electronic control device; (Nakano fig. 2 A # 14) and a connecting part, (Nakano fig. 2A #22) wherein the ground wiring pattern is connected to the output voltage forming circuit and defines a ground electrical potential of the output voltage forming circuit, ; (Nakano figure 2 A col. 3 lines 65-67) the common ground wiring pattern is formed in a multi-layered substrate (Nakano fig. 4a , col. 4 line 59 –col.5 line 5) and defines a ground electrical potential of each electronic circuit, (Nakano claim 4, etc.) and the connecting part is provided for connecting the ground wiring pattern.

The recitation, the connecting part is provided for connecting the ground wiring pattern is taken to be inherent functional recitation. See In re Swinehart, 169 USPQ235 (CCPA 1971).

Also , "the connecting part is provided for connecting the ground wiring pattern" to be given patentable weight must be expressed as a " means " for performing the specified function, as set forth in 35 USC 112, 6th paragraph and must be supported by recitation in the claim of sufficient structure to warrant the presence of the functional language. In re Fuller, 1929 C.D. 172, 388 O.G. 279.

With respect to claim 2 Nakano describes the electronic control device according to claim 1, wherein: the output voltage forming circuit includes a smoothing circuit constructed of a choke coil and a capacitor, (Nakano figure 3 below 300 – choke coil and #11 –buffer amplifier- acts as capacitor) and a freewheel component (figure 4a #19, etc.) connected in parallel with the smoothing circuit for feeding a current back to the choke coil when the switching component is turned off; and the smoothing circuit and the freewheel component are connected to the ground wiring pattern of the output voltage forming circuit.

The recitation, "for feeding a current back to the choke coil when the switching component is turned off "is taken to be inherent functional recitation and for reasons set out above under calim1 and incorporated here by reference not given patentable weight.

With respect to claim 3 Nakano describes the electronic control device according to claim 2, wherein the ground wiring pattern between the smoothing circuit and the freewheel component has impedance lower than that of the connecting part. (Nakano col. 4 lines 28-32).

With respect to claim 4 Nakano describes the electronic control device according to claim 1, wherein: the output voltage forming circuit further includes an input-side smoothing circuit constructed of a choke coil and a capacitor and a terminal of which is connected to an input terminal of the switching component; (Nakano figure 3 #200) the power supply voltage is applied to the input terminal of the switching component after smoothed out by the input-side smoothing circuit; (Nakano claim 1 –input terminal) and

the ground wiring pattern is connected to another terminal of the input-side smoothing circuit. (Nakano figure 4A).

With respect to claims 5 and 6 Nakano describes the electronic control device according to claim 1, wherein: the ground wiring pattern is formed in a top layer of the multi-layered substrate; and the connecting part is configured as an interlayer connecting part (Nakano fig. 4a , col. 4 line 59 –col.5 line 5) for connecting the ground wiring pattern formed in the top layer of the multi-layered substrate and the common ground wiring pattern formed in an inner layer of the multi-layered substrate via interlayer connection.

The functional recitation "for connecting the ground wiring pattern formed in the top layer of the multi-layered substrate and the common ground wiring pattern formed in an inner layer of the multi-layered substrate via interlayer connection" is not given patentable weight for reasons set out above.

With respect to claim 7 Nakano describes the electronic control device according to claim 1, wherein the connecting part has a via hole through which the ground wiring pattern is connected with the common ground wiring pattern. (Nakano col. 5 line 2).

With respect to claims 8 and 9 Nakano describes the electronic control device according to claim 1, wherein the connecting part has a through hole having a conductive material inside through which the ground wiring pattern is connected with the common ground wiring pattern. (Nakano col. 5 lines 1-5).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (571) 272-1718 . The examiner can normally be reached on 8.00 to 5.00.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven H. Rao
Patent Examiner
October 15, 2004.

PHAT X. CAO
PRIMARY EXAMINER